Analysis of charge transport in a polycrystalline pentacene thin film transistor by temperature and gate bias dependent mobility and conductance

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The gate bias and temperature dependent field-effect mobility and conductance of a polycrystalline pentacene thin film transistor (TFT) were analyzed to study the charge transport in the material. Since both heating and cooling can obviously change the film morphology, a relatively narrow temperature range was adopted to rule out the possible influence of structure variation on the device characterization. Both mobility and conductance values increased with the gate bias and showed a thermally activated Arrhenius-like behavior, while the threshold voltage decreased with temperature. Several models were compared, and it was found that the observations could only be well interpreted by a multiple trapping model, which suggests that the temperature and gate bias dependences should be attributed to the increased free charge carrier density. The density of trap states in the band gap was evaluated by the field-effect mobility as well as the field-effect conductance data. The results disclose a possible field-effect mobility much higher than the present record in a polycrystalline pentacene TFT. © 2007 American Institute of Physics. [DOI: 10.1063/1.2753671]

I. INTRODUCTION

Organic thin-film transistors (OTFTs) based on conjugated polymers, oligomers, or other molecules have been envisioned as a potential alternative to more traditional, mainstream inorganic TFTs for more than a decade. Despite the much lower mobility of organic semiconductors than that of inorganic ones, the processing characteristics and the demonstrated performance of OTFTs suggest that they are competitive for TFT applications requiring large area, flexibility, low-temperature processing, and low cost. It is well known that the band-type transport in crystalline inorganic semiconductors is limited by the scattering of the carriers by phonons and the charge mobility decreases with temperature. However, owing to the large number of defects, the transport controlled by localized trap states in polycrystalline organic semiconductor films is much more complicated. On the other hand, the quality of the vacuum deposited organic films is very sensitive to various parameters, such as temperature, deposition rate, pressure, chemical purity, and the substrate surface conditions. As a result, the performance of OTFTs depends crucially on the fabrication procedure because of the different crystallinity, grain size, and amount of defects in the films prepared from run to run. Due to these reasons, various results of thermally activated,1 thermally deactivated,2,3 as well as temperature independent4 field-effect transport have been reported. It seems that the detailed correlation between the structural disorder and the transport in organic semiconductors is not fully understood, although much is known about the role of structural disorder in inorganic semiconductors.

Pentacene is one of the most promising organic semiconductors due to its stability and reproducibly obtainable high mobility of ~2 cm2 V−1 s−1.5 In this study the temperature and gate voltage ($V_g$) dependence of field-effect mobility $\mu$ and field-effect conductance $\sigma$ of a pentacene TFT were analyzed to understand the transport properties. Since the performance of OTFTs is strongly dependent on numerous factors, to achieve an accurate analysis, here special attention was paid to several important issues, i.e., the TFT architecture, the ambient atmosphere, the film thickness, and the temperature range.

Although several methods can be used to evaluate the influence of contact resistance, presently an accurate estimation seems still very difficult. It is well known that TFTs with bottom contact (BC) electrodes have a much higher contact resistance than that of the top contact (TC) ones. Therefore, the TC architecture was adopted to minimize the contact resistance. TC architecture also removes the possible influence of Au electrode patterns on the growth of pentacene films associated with a BC one. Exposure to atmosphere was also found to cause gradual deterioration of the pentacene TFT performance even at room temperature (RT), and the deterioration was $V_g$ dependent.6 Hence, the device was characterized in a high vacuum to rule out the possible influence of thermal oxidation on the temperature and gate bias dependence. In addition, despite the importance of temperature induced structural variation and film thickness, these factors seem to have rarely been discussed so far. Resulting from the weak van der Waals intermolecular forces, organic molecules, especially nonpolar ones, have much lower cohesive energy compared to inorganic ones. In particular, pentacene was reported to have a relatively low melting point in the polyacene sequence.7 Our previous atomic force microscopy
(AFM) and x-ray diffraction (XRD) results have confirmed that heating above a temperature of 45 °C (depending on the deposition and TFT characterization conditions) can cause deteriorated morphology and decreased degree of order. On the other hand, cooling may cause grain cracking due to the huge mismatch in the thermal expansion coefficients of the organic film and the SiO₂ substrate. Cooling may also induce sample shattering, change in the ratio of different polymorphs, and even phase transition. These indicate that the charge transport characterization may be significantly affected by both heating and cooling. Thus, it seems indispensable to select a suitable temperature range, so that the influence of film structure variation on the device performance can be neglected. Therefore, a relatively narrow temperature range of RT to 45 °C was selected in this study. Actually, a high temperature roll off in the Arrhenius plot of mobility has been reported before for OTFTs, which may probably be due to the structural deterioration. Our preliminary test also observed a roll off at above ~60 °C in the Arrhenius plot of mobility of the samples when a higher temperature was used. Thus, the linear Arrhenius plot (see Fig. 6) indicates that the influence of the thermally induced structural deterioration is negligible in the temperature range used here. Regarding the film thickness, we found that the drain current \( I_d \) showed a maximum at a certain thickness value depending on the gate bias. The fundamental cause of the phenomenon, though still unclear, may affect the variable temperature and gate voltage characterization. Thus, the film thickness was selected according to a thickness dependence study.

II. EXPERIMENT

Heavily doped n-type silicon wafers with a 300 nm thick thermally grown SiO₂ dielectric layer were used as the substrates, which were cleaned by acetone before use. Pentacene powder from Aldrich Chemical was used without further purification to deposit films at RT by vacuum sublimation at a pressure of \( \sim 10^{-5} \) Pa. The film thickness was monitored with a quartz crystal microbalance. For the film thickness dependence test, an \textit{in situ} electrical characterization based on the same BC TFT sample was conducted during the film deposition. Thus, the performance variation due to film quality difference was excluded. For the temperature and gate bias dependent characterization, a TC sample was used, i.e., 30 nm gold source and drain electrodes were deposited on top of the pentacene film through a shadow mask. The channel length and channel width of the sample are 0.1 and 5.4 mm, respectively. The influence of contact resistance is expected to be negligible with this relatively large channel length, while it may be significant for a channel length close to 10 \( \mu \)m. The sample temperature was measured by a Chromel-Alumel thermocouple. The electrical characteristics of the TFT were measured in a high vacuum with a pressure of \( \sim 10^{-5} \) Pa by Keithley 487 picoammeter/voltage source units after achieving stabilized temperatures. Film morphology was inspected by a JEOL JSPM-5200 AFM operated in tapping mode.

III. RESULTS AND DISCUSSION

A. Thickness dependent device performance

Although it is well accepted that charge transport in a single grain mainly occurs in the beginning 1 or 2 ML (1 ML \( \sim 1.5 \) nm), it is evident that the effective channel is far beyond the initial several monolayers in a thick polycrystalline film and the dependence of the device performance on the film thickness is still a matter of debate. We have repeatedly tested the thickness dependence of \( I_d \) and mobility, and the typical plots are shown in Fig. 1. We can see that \( I_d \) and the saturation mobility \( \mu_s \) reach a maximum at 20–25 ML, then decrease slightly but clearly with increasing thickness. The appearance of maximum \( I_d \) and mobility at a certain thickness has also been reported in a BC CuPc TFT (Ref. 16) and in both BC and TC pentacene TFTs, even after contact resistance correction. Although the exact reason is still unclear, our recent Kelvin force microscopy of an operating OTFT indicated that the maximum \( I_d \) thickness was closely related to the potential and charge distribution along the surface normal, and it might be affected by the gate bias. As a result, the physical reason beneath the phenomenon may probably affect the temperature and gate bias dependences of transport. We can see from the inset AFM images that the
sample of Fig. 1(b) has a larger grain size and a lower roughness value than the sample prepared with a much higher deposition rate shown in Fig. 1(a). This morphology difference may account for the relatively higher maximum \( I_d \) thickness of Fig. 1(b) than that of Fig. 1(a). Therefore, according to Fig. 1(b) we selected a film thickness of 40 nm for the transport study sample, which was prepared with an identical deposition rate of \( \sim 0.6 \text{ nm/min} \). At such a thickness, stable \( I_d \) and mobility can be obtained and a characterization just on the active conducting layers may be achieved.

### B. Temperature and gate bias dependences of field-effect mobility and conductance

The voltage distribution in transistors is controlled by two independent biases, and the voltage drop through the insulator is not the same at the source and at the drain. Therefore, if the mobility is gate bias dependent, it will vary all along the conducting channel and will be difficult to be determined. Hence, in order to investigate the gate bias dependence, we used the linear region mobility derived from the transconductance \( g_m \) at different gate voltages through

\[
g_m = \left. \frac{\partial I_d}{\partial V_g} \right|_{V_g=-1V} = \frac{W}{L} \mu C_i V_d,
\]

where \( W, L, C_i \) and \( V_d \) represent channel width, channel length, capacitance of the insulator, and drain voltage, respectively. By using a very low \( V_d \) of \(-1 \text{ V} \), mobilities practically constant all along the channel were expected. Another issue that needs to be noted is that the contact resistance should be considered to evaluate the gate bias dependence. However, since the contact resistance may also be gate bias dependent, \(^{13,18,21,22} \) it is very difficult to calculate the mobility by introducing an additional independent variable. The problem inherently associated with the resistance (\( R \)) versus channel length (\( L \)) plot method is the film quality variation from run to run. An improved four-probe method was applied to OTFTs, \(^{9,23} \) while the contact resistance in this method is derived from a linear extrapolation of the channel potential; thus, the accuracy of the method may be sensitive to the device preparation conditions. It was also reported that the contact resistance might depend not only on the contact area but also on the details of the electronic structure at the pentacene/dielectric interface. \(^{22} \) Due to these reasons, accurate evaluation of the contact resistance seems still very difficult, and substantially different gate bias dependences have been reported. \(^{9,13,18,21} \) Therefore, in this study \( g_m \) was used to derive the \( V_g \) dependent mobility. Importantly, here six TFT samples were tested. The linear mobilities at \( V_g=\pm 50 \text{ V} \) were found to vary between 0.09 and 0.33 \( \text{cm}^2 \text{V}^{-1} \text{s}^{-1} \), while three samples showed very similar mobilities of 0.29, 0.31, and 0.33 \( \text{cm}^2 \text{V}^{-1} \text{s}^{-1} \), which were close to the present record of polycrystalline pentacene TFT on untreated SiO\(_2\) surface. Therefore, the sample with the highest mobility of 0.33 \( \text{cm}^2 \text{V}^{-1} \text{s}^{-1} \) was used for analysis. This method is simple, though not ideal, and we found that the results were in good agreement with the prediction by the multiple trapping model.

A considerable curvature is present in the plots of \( I_d \) vs \( V_g \) shown in Fig. 2. We can see from the calculated data in Fig. 3 that \( \mu \) increases with \( V_g \) and gradually saturates at high \( V_g \) region. This is very similar to the \( V_g \) dependence of contact corrected mobility obtained on a TC pentacene TFT using the four-probe method \(^{18} \) and the computed simulation of an amorphous silicon TFT, \(^{24} \) indicating that the influence of contact resistance of the sample is negligible. For a further confirmation, the gate bias dependence of the saturation mobility \( \mu_s \) of the sample obtained at \( V_d \) of \(-60 \text{ V} \) is also plotted in Fig. 3. It may be easily understood that the linear regime is more strongly affected by contact resistance than the saturation regime. Any voltage drop across the source drain electrode/semiconductor interfaces due to contact resistance has only a relatively smaller effect on the saturation regime than on the linear regime, since in the saturation regime the drain current is already independent of the drain voltage. A similar character can be seen in Fig. 3 for the curve of \( \mu_s \), which further confirmed the negligible influence of contact resistance and the \( V_g \) dependence of carrier mobility.
The output characteristics are shown in Fig. 4. The conductance values were derived from $dI_d/dV_d$ of the output curves at $V_d=0$ V so that the influence of the depletion region at the drain side at high $V_d$ was avoided. $V_g$ dependence of the derived conductance data at different temperatures is shown in Fig. 5, which is similar in shape with Fig. 3, implying that a similar $V_g$ dependence of $\mu$ can be found if the conductance data were used to calculate $\mu$. The logarithmic mobility and logarithmic conductance versus reciprocal temperature of the polycrystalline pentacene TFT are shown in Figs. 6(a) and 6(b), respectively. We can see that both the mobility and the conductance exhibit an Arrhenius-like behavior in the tested temperature range.

Several models may be used to explain the gate bias and temperature dependent results of the sample, including a Poole-Frenkel (PF) effect, a modified variable range hopping (VRH) model based on the percolation theory, and a model based on the concept of multiple trapping (MT) and thermal release with an exponential density of states (DOS). PF model considers that the emission from the traps, hence the mobility, is dependent on the longitudinal electric field $E_L$ caused by the source drain voltage. VRH model is based on a large number of traps. In the classic VRH model, the transport occurs by hopping from one site to another and is limited by the wave function overlap as well as the barrier height. The temperature dependence is a consequence of hopping over far distances and hopping to high energies being equally important. In the modified VRH model, transport occurs also by carrier hopping, while the model describes the conductivity as equivalent to transport through a resistor network where the nodes of the network have different energies according to the exponential DOS. The percolation criterion through the network is related to the temperature, the Fermi level $E_F$, and the width of the exponential tail of the DOS. The MT model is also based on a large number of traps, but it invokes a mobility edge. It assumes that charge transport is dominated by recurrent trapping into localized (zero mobility) “trap” states above a mobility edge (for holes) followed by thermal activation into delocalized states below the mobility edge.

According to the PF law, there is a field dependent mobility,

$$\mu = \mu(0)\exp\left[-\frac{q(\Phi_B - \sqrt{qE_F/e})}{kT}\right],$$

where $\mu(0)$ is the zero field mobility, $q$ is the elementary charge, $\Phi_B$ is the trap depth, $e$ is the semiconductor permit-
tivity, and $k$ is the Boltzmann constant. Equation (2) implies a superlinear relationship between $I_d$ and $V_g$ at small $V_g(E_d=V_g/L)$ region of the output curves. However, no such nonlinearity can be discerned in Fig. 4 even if a small $V_g$ step of $-2$ V was used, indicating that a PF effect should not dominate in the tested temperature range.

VRH model predicts a linear variation of $\ln \mu$ as a function of $T^{-1/4}$, thus, the Arrhenius relationship of both $\mu$ and $\sigma$ shown in Fig. 6 excludes the possibility of a classic VRH-type transport in the sample. While the modified VRH model based on the percolation theory also predicted an Arrhenius-like behavior for both $\mu$ and $\sigma$. To check the applicability of this model, we use an empirical relationship \cite{24,26,28} for the linear region of the TFT sample,

$$I_d = \frac{W}{L}C_d\mu(V_g-V_t)^{1+\gamma}V_g,$$

where $V_t$ is the threshold voltage and $\gamma$ is a parameter that indicates the deviation from the standard field-effect transistor (FET) theory. The modified VRH model calculates a mobility of the following form:

$$\mu = \frac{\sigma_0}{\varepsilon} \left[ \frac{\pi(T_0/T)^3}{(2\alpha^3)B_\gamma \Gamma(1-T_0/T)\Gamma(1+T_0/T)} \right]_{T_0/T}$$

where $\sigma_0$ is the conductivity prefactor, $\alpha$ is the wave function overlap parameter, $T_0$ is a parameter describing the slope of the distribution of DOS, $\Gamma(\varepsilon)=\int_0^\infty \exp(-\gamma)\gamma^{\alpha-1}d\gamma$, and $B_\gamma$ is a constant. Compared with Eq. (3), Eq. (4) implies a temperature dependent $\gamma=2(T_0/T)-3$. The $\gamma$ can be derived through the plot of $\ln I_d$ vs $\ln(V_g-V_t)$. As can be seen in Fig. 7, the curves for different temperatures show a same slope of 2, implying a $T$ independent $\gamma$ of 1. Therefore, the modified VRH transport can also be ruled out. Interestingly, a constant $\gamma$ value of 1 agrees very well with Shur’s computed simulation of amorphous silicon TFT based on the MT concept.\cite{24,26,28} Since there are numerous types of traps in the polycrystalline pentacene film, the gate voltage induced charge can be separated into two parts: the trapped carriers and the free carriers. We can assume a value $\theta$ as the ratio of free carrier density $N_f$ to the total carrier density $N$ induced by $V_g$. Based on the relationship $\sigma=N_f\mu_0=N_f\mu_0\theta$, the as-measured $\mu$ data in Fig. 3 may be seen as effective values that are equal to the product of the free (intrinsic) carrier mobility $\mu_0$ and the free carrier ratio $\theta$. Following the MT model,\cite{24,29} there is an exponential dependence of both the density of trapped charges $N_t$ and $N_f$ on the position of the $E_F$.

$$N_t = N_{t0} \exp(-aE_F),$$

$$N_f = N_{f0} \exp(-bE_F).$$

Due to the polycrystalline nature of the film and according to Shur’s calculation, a $N_{t0}$ of 1 (i.e., $b/a=2$) reflects that $\theta=1$. Thus, considering that $C_dV_g=V_f+N_f$, a combination of Eqs. (4) and (5) gives the following equation:

$$I_d \propto C_dV_g^{b/a}V_g = C_dV_g^2V_g.$$

The gate bias dependence of $\mu$ can be seen by comparing Eq. (7) with Eq. (3). Equation (7) may also explain the general character of the $V_g$ dependent $I_d$ shown in Fig. 2. These imply that the $V_g$ dependence of the as-measured mobility $\mu$ may seem to result from the increased total free carrier density.

If we extend the lines of the Arrhenius plots to high temperature, we can find that all lines in Figs. 6(a) and 6(b) approximately intersect at a single crossing point at $1/T = 0$ (not shown in the figure), indicating that the Meyer-Neldel rule (MNR) is applicable to the sample. It has been established that multi-trapping-dominated quantities always exhibit the MNR.\cite{30} Hence, the appearance of the MNR provides a further evidence of a MT-type transport of our sample.

From the slopes of the Arrhenius plots, the activation energy for both the mobility $E_{\mu}$ and the conductance $E_{\sigma}$ were calculated and the data are listed in Table I. It is apparent from Table I that both $E_{\mu}$ and $E_{\sigma}$ decrease with the increasing $V_g$, and they show similar values and $V_g$ dependence. The activation energy $E_{\sigma}$ depends on the surface potential and may be approximately taken to be the difference in energy between the valence band edge $E_g$ and the Fermi level $E_F$ at the surface.\cite{31} Thus, the decrease of $E_{\sigma}$ with increasing negative $V_g$ may be seen as a direct result of the decrease of $E_F - E_g$. As $V_g$ increases, carriers in the system have an average higher energy and the Fermi level moves closer to the band edge, causing an increased free carrier density and hence an increased $\mu$. The $V_g$ dependence of $\mu$ shown in Fig. 3 is in good agreement with Shur’s calculation of an increased but gradually saturated (due to trapping) total free carrier density.

<table>
<thead>
<tr>
<th>$V_g$ (V)</th>
<th>$-60$</th>
<th>$-50$</th>
<th>$-40$</th>
<th>$-30$</th>
<th>$-20$</th>
<th>$-10$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{\mu}$ (meV)</td>
<td>57</td>
<td>80</td>
<td>90</td>
<td>102</td>
<td>111</td>
<td>113</td>
</tr>
<tr>
<td>$E_{\sigma}$ (meV)</td>
<td>57</td>
<td>71</td>
<td>72</td>
<td>84</td>
<td>94</td>
<td>103</td>
</tr>
</tbody>
</table>

TABLE I. List of activation energy $E_{\mu}$ and $E_{\sigma}$ at different $V_g$. |
FIG. 8. Levinson plots of two curves with different $V_g$ range tested at RT.

with increasing $V_g$, indicating a transport controlled by charge production and subsequent trapping in the pentacene TFT.

In addition, the grain boundary barrier model also predicts a $V_g$ dependent mobility, $\mu = \mu_0 \exp(-kT/E_b)$, $\mu_0 \exp(-s/V'_g)$, where $E_b$ is the energy barrier, $s$ is a parameter related to the grain boundary charge, and $V'_g$ is $V_g$ corrected by a voltage close to $V_t$. According to this model, charge states at the grain boundary present an electrostatic barrier to carrier transport, but charges within the grain screen the potential, reduce the barrier, and increase the effective mobility. This model predicts that a Levinson plot of $\ln(I_d/V'_g)$ vs $1/V'_g$ results in a straight line. However, the Levinson plots of our sample shown in Fig. 8 are far from being straight lines. Therefore, this model may not be applied to explain the $V_g$ dependent transport of the pentacene TFT. Figure 8 may also indicate that the grain boundaries are traps rather than barriers.

The transfer characteristics of the sample and the threshold voltage $V_t$ derived by fitting the linear part of the transfer curves are shown in Fig. 9. We should note that several types of plots have been used to derive the $V_t$ values in literature, including the $V_g$ dependence of $I_d$, $\sigma$, and $\sqrt{V_t}$, may be seen as the gate voltage at which the conducting channel starts to form. The $|V_t|$ values derived from $I_d$ and conductance plots are larger than 20 V (not shown), which is not realistic because conduction in our sample actually occurred at much smaller $V_g$. Therefore, here the $V_t$ dependence of the square root of $I_d$ was used to derive the $V_t$ values. The $V_t$ in inorganic FETs is used to derive the $V_t$ value. The $V_t$ in organic FETs (OFETs) operate not in the inversion regime but in the accumulation regime through the vertical gate field, the $V_t$ should be very small. However, a high $V_t$ is generally observed in OFETs, indicating that the $V_t$ has a physical cause different from that of an inorganic FET. The observed $V_t$ may seem to result from the voltage drop at the insulator semiconductor interface, the bulk conductivity of the semiconductor layer, and the flatband potential $V_{FB}$, which originates from any kind of energy level misalignment at both sides of the insulator. As a special source of energy level misalignment, surface dipole moments induced by self-assembled monolayers may introduce additional built-in electric field between the semiconductor and the dielectric and hence significantly shift the $V_t$ value. While the reported $|V_{FB}|$ for pentacene FETs on SiO$_2$ without surface treatment layer is very small, all these contributions to $V_t$ should be much smaller than the data in the inset of Fig. 9. Therefore, the $V_t$ data (or more precisely the curvature in the low $V_g$ region of the transfer curves) of our sample may seem to mainly come from the trap limited charge transport; i.e., a higher $V_g$ is required to fully form a conducting channel. In addition, Fig. 9 indicates that the $V_t$ decreases with temperature, and a same dependence can also be found if $V_g$ dependence of $I_d$ or $\sigma$ are used for deriving $V_t$. Based on the Arrhenius behavior, i.e., $\sigma = A \exp(-E_{\sigma}/kT)$ and $\mu = B \exp(-E_{\mu}/kT)$, the following relationship can be obtained:

$$C_i(V_g - V_t) = \frac{\sigma}{\mu} = \frac{A}{B} \exp[-(E_{\sigma} - E_{\mu})/kT].$$

where $A$ and $B$ are constants. Table I indicates that $E_{\sigma}$ is larger than $E_{\mu}$ except at $V_g = -10$ V. Therefore, it may be qualitatively estimated from Eq. (8) that the increase of $T$ decreases the $V_t$, and hence the temperature dependence of $V_t$ may be attributed to the thermally activated transport nature and may be explained in terms of trapping and thermal activation of the free charge carrier density. An increase in temperature shifts the mobility edge, which is caused by an increased emission rates (or a decreased trapping time) for charges in the tail states of the band gap. The microscopic origin of the traps on devices with a SiO$_2$ dielectric layer was reported to be closely related to molecular layers of water adsorbed on the SiO$_2$ surface, which is normally composed of hydrophilic hydroxyl groups. This may be a general origin of traps in the devices since thin layers of water may be present on SiO$_2$ even under high vacuum and thus trapped at the interface when pentacene is deposited.
C. Evaluation of DOS in the band gap

Based on a MT-type transport model, the DOS in the band gap can be roughly estimated from the temperature dependent field-effect mobility data.\(^{39}\) According to the foregoing result of \(b/a=2\), we may assume that most of the carriers are trapped. Thus, we have the approximation \(N=N_f\) at equilibrium, the surface potential, the transport band edge, respectively. Considering that the energy at equilibrium, the surface potential, the transport band edge, respectively. Considering that the Fermi distribution \(f(E)\) with a step function, the DOS can be approximated by

\[
N_f(E) = q \frac{dN_f}{dE} = \frac{d(C_sV_g)}{dE}.
\]

Using the product \(\mu_0N_c\) as an adjustable parameter, \(E_F\) can be determined from Eq. (10). Then \(N_f(E)\) can be estimated by a numerical derivation of the product \(C_sV_g\) as a function of \(E_F\). For our sample, the best agreement of the data at different temperatures was obtained with \(\mu_0N_c = 10^{13} \text{ V}^{-1} \text{ s}^{-1}\). The area DOS can be converted into a volume density by selecting a depth over which the carriers are trapped. From our thickness dependent results a depth larger than 30 nm should be adopted. Since the DOS decreases from the interface to the bulk, here a depth value of 10 nm was used. The result is shown in Fig. 10, which indicates an exponential distribution of DOS in the band gap.

The DOS in the band gap can also be estimated from the simultaneously obtained conductance data by the so-called field-effect conductance (FEC) method,\(^{41}\) which was reported to be able to calculate \(N_f(E)\) with a theoretically reasonable degree of accuracy. Based on a one-dimensional Poisson’s equation, the DOS in the FEC method is given by

\[
N_f(E_F + \psi_s) = \frac{\varepsilon}{2q} \left( \frac{d\psi_s}{dx} \right)^2, \tag{13}
\]

where \(\psi_s\) is the band bending at the semiconductor/dielectric interface (where \(x=0\)). The electric field at the interface is given by

\[
\frac{d\psi}{dx} \bigg|_{x=0} = -\frac{\varepsilon_d}{\varepsilon_p} \frac{d\psi}{d\mu} = -\frac{\varepsilon_d V_g - V_{fb} - \psi_s}{\varepsilon_p} \tag{14}
\]

where \(\varepsilon_d\) and \(d\mu\) are the permittivity and thickness of the \(\text{SiO}_2\) layer, respectively. After numerical determination of the relationship between \(V_g\) and \(\psi_s\) by the “temperature method,”\(^{42}\) from the conductance data, the DOS can be derived from Eqs. (13) and (14). A precise estimation of \(V_{fb}\) seems very difficult, especially when it is very small for pentacene TFTs.\(^{28}\) Because at the switch-on voltage there is no band bending, \(V_{fb}\) might be seen as the switch-on voltage. As relatively high gate voltages were used, \(V_{fb}\) was neglected. The final result is also shown in Fig. 10. The curvature of the plot and the discrepancy with the FET method may mainly be due to the errors caused in calculating the second derivative of \(\psi_s\). Nevertheless, the broad features can be illustrated, and it seems qualitatively consistent with the \(N_f(E)\) estimated from the field-effect mobility method, indicating a very large density of traps in the pentacene TFT.

If the effective DOS is taken as one state per molecular, \(N_c\) can be estimated from the molecular density of pentacene (2.9 × 10\(^{21}\) cm\(^{-3}\)). By converting this value to an area density of states with a thickness of 1 ML of 1.5 nm, we can find that \(N_c\) is in the order of 10\(^{14}\) eV\(^{-1}\) cm\(^{-2}\). Thus from \(\mu_0N_c = 10^{13} \text{ V}^{-1} \text{ s}^{-1}\) estimated from Fig. 10, the free carrier mobility may be estimated to be 0.1 cm\(^2\) V\(^{-1}\) s\(^{-1}\), which seems too small to be realistic. However, it should be noted that \(N_c\) is generally much smaller than the molecular density. It has been established that \(N_c\) at the conduction level is strongly influenced by the crystalline structure of the samples. The \(N_c\) in oriented organic layers could be several orders of magnitude lower than that in single crystals, and the \(N_c\) in polycrystalline films could be several orders of magnitude lower than that in oriented layers.\(^{33}\) Therefore, the estimated \(\mu_0\) of 0.1 cm\(^2\) V\(^{-1}\) s\(^{-1}\) based on a \(N_c\) estimated from the density of molecules in pentacene single crystal is the minimum limit, while \(\mu_0\) may actually be several orders of magnitude higher. Also for a rough estimation of \(\mu_0\), we found through the MNR that all lines in Fig. 6 approximately intercepted at the same ln \(\mu\) value of \(\sim 2\), corresponding to a mobility value of
~8 cm² V⁻¹ s⁻¹ for the high temperature limit. This value is almost the same with the highest mobility reported so far for a single crystal rubrene FET.⁴⁴ It is notable that even purified single crystals were reported to have broadband tails due to the unavoidable various defects, especially near the gate dielectric interface.³¹ These indicate that it is possible to obtain an exceptionally higher mobility in OTFT, provided that the defects in the semiconductor film are substantially removed.

IV. CONCLUSION

We investigated the temperature and gate bias dependence of transport of a pentacene TFT in a vacuum in a narrow temperature range near RT after careful selection of the film thickness. The field-effect mobility and the conductance of the same device were characterized and both values showed an Arrhenius-like behavior. The threshold voltage was found to decrease with the temperature. These indicate a thermally activated transport of the organic film, which can be explained by neither the classic VRH model nor the modified VRH model. However, due to the polycrystalline nature of the pentacene film, the results can be well explained by a MT-type model. Accordingly, the $V_{th}$ and temperature dependence of mobility and the conductance can be attributed to the increased total free carrier density. The DOS in the band gap was evaluated by a field-effect mobility method and compared with the calculation by a FEC method. The result reveals a very large density of traps in the pentacene film. It also implies that it is possible to obtain a significantly higher mobility in organic semiconductors once the defects in the materials are substantially removed.

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